International Journal of Electrical and Electronics Engineering Research (IJEEER) ISSN(P): 2250-155X; ISSN(E): 2278-943X Vol. 4, Issue 1, Feb 2014, 119-124 © TJPRC Pvt. Ltd. TRANS
STELLAR
Journal Publications - Research Consultancy

# CAPACITANCE EXTRACTION USING MONTE CARLO METHOD

# HEMRAJ V. DHANDE<sup>1</sup> & P. M. MAHAJAN<sup>2</sup>

<sup>1</sup>Scholar, Department of Electronics and Telecommunication, J.T.M.C.O.E, Faizpur, Maharashtra, India <sup>2</sup>Associate Professor, Department of Electronics and Telecommunication, J.T.M.C.O.E, Faizpur, Maharashtra, India

#### **ABSTRACT**

Recent trend for Designing of Integrated Circuits (ICs) used the Very Large Scale Integration (VLSI) technology. The VLSI chips designed with micro level transistors or MOFET uses interconnections according to the function of ICs. The number of parameters which effects on the performance and efficiency of the ICs like Capacitance, Inductance and Resistance between the interconnect conductors. Extraction of these parameters can improve the speed and performance of these ICs. This paperfocuses on the parasitic capacitance mainly as self and mutual capacitance produced between interconnects and ground plane and between two interconnect metals respectinely and extraction of this capacitance is main task. In thiswork the Monte Carlo based capacitance extraction method is used which followes by the random walk process. Experimentations are performed on 10 nets and extract the produced capacitance, detail of methods and results of this capacitance extraction are discussed in detail.

**KEYWORDS:** Monte Carlo, Random Walk, Capacitance Extraction

## INTRODUCTION

In this High-speed Era all things around us are Digital. Recents cenario is focused on development of smallest and powerful computational Digital ICs. Digital ICs contain small interconnect paths for inter device connection. Performance and efficiency of this digital ICs depends on capacitance produced between this interconnected paths. Self and coupling capacitances both play important rolein the micron layout swith in ICs. Accurate computation of this capacitance is the key to success of signal timing analyses. Reduction of both capacitances will improve the performance of circuit or chip.

Various researchers [1-4] detailed different techniques for computation and reduction of the interconnect capacitance [1-4]. Various numerical techniques like Boundary Element Method (BEM)[1,6], Finite Element Method (FEM) [4], Monte Carlo Integration [3], etc. which can compute these capacitances at different levels of accuracy. In this Paper we focused on Monte Carlo integration followed by variance reduction techniques. Monte Carlo methods compute capacitance by evaluating the charge integral by statistical sampling techniques [8,9]. The statistical sampling is implemented through random walk process [3].

The BEM relates the potential at the conductor boundaries to the charge distribution at those boundaries [1], BEM discretize boundary and volume in to elements, and write electro static equations at each element. The resulting linear equations are solved by efficient techniques. Boundary element based field solvers can effectively be used for small structures but can not used for large structures because of large grid requirement [2]. The Finite element method (FEM) is a numerical method for solving a differential or integral equation. This method essentially consists of assuming the piece wise continuous function for the solution and obtaining the parameters of the functions in a manner that reduces the error in the solution.

### **METHODOLOGY**

Monte Carlo is the one of the efficient method for extraction of capacitance produced in interconnects of the VLSI chip or IC[3,10,11]. The Monte Carlo algorithm utilizing multiplication, tracing and computation. Monte Carlo method computes capacitance by evaluating the charge integral by statistical sampling techniques. The statistical sampling is implemented through random walk process. A random walk starting from a point on a Gaussian surface of a net and then goes through several random hops before terminating on another conductor [5]. Since the random walks are completely independent of eachother, could be carried out in parallel in order to achieve the speed improvement. The detail scheme of Methodology for capacitance extraction using Monte Carlo algorithm are described in brief as,

• To find the capacitances in the conductor decide the target conductor which is called as nets. Here10 conductors are used for experimentation with ground plane, as shown in Figure 1.

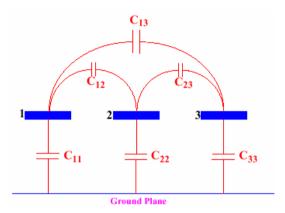


Figure 1: Self and Mutual Capacitance between Conductors

- Capacitance is defined by C=QV sowe have to find the charge Q on the conductor for self capacitance and linear charge between two conductor for mutual capacitance. Keep voltage at V=1 volt.
- Apply Gauss's law to find Q on the conductor for self capacitance with reference to ground plane. Gauss law
  relates capacitance (total charge on conductor) to integrated electrical field around the conductor according to
  equation no 1.

$$C=\int E \cdot ds(1)$$

- Apply Green's function to computes the potential for boundary region on conductor. Green's function relates the
  E strength (derivative of potential) to potential over the boundary. We can measure electrical field by random
  point sample of potential.
- Random Walk process is applied on different points to estimates the potential according to the mean value
  theorem of electrostatics which states the potential of any point is equal to the mean potential of all points on a
  spheresur rounding that point[7]. This theorem can be extended to weighted samples over any closed geometry,
  like a cube.
- By selecting the random point from one conductor and calculating the potential of that point with considering cube centered on that selected point with help of mean value theorem of electrostatics.
- Find the different points potentials by random walk process until we find the overall potential between the two conductors and that is the mutual capacitance between that two interconnect metals.

#### RESULTS AND DISCUSSIONS

The detailed capacitance extraction is implemented using Linux Cent OS-6.5, x86\_64 with packages yum install gcc-c++, yum install glibc.i686, yum install libstdc++. i686 to perform our experiment. Figure 2 shows all input parameters are provide to the system. The specification of 10 conductors named from METAL\_0 to METAL\_9 and one Dielectric plane and one ground plane with its specified dimensions as shown in Figure 3.

```
Wed Jan 8, 5:55 PM dhande
  Applications Places System 🍪 🕝 🗾
                                                                                   hemraj@localhost:~/Desktop/EXCTRACT_11/rundir
  File Edit View Search Terminal Help
File Edit View Search Terminal Help
[hemraj@localhost ~]$ cd Desktop
[hemraj@localhost Desktop]$ cd EXCTRACT_11
[hemraj@localhost EXCTRACT_11]$ cd c
[hemraj@localhost c]$ make clean
rm -f extract geomutils.o gfdb.o captomc.o qtree.o mcextract.o net.o *~
[hemraj@localhost c]$ make all
g++ -03 -c geomutils.c
g++ -03 -c gfdb.C
g++ -03 -c mcextract.c
g++ -03 -c net.C
a++ -03 -c of tree.C
g++ -03 -c net.C
g++ -03 -c qtree.C
g++ -03 -c captomc.C
g++ -03 - o extract gfdb.o qtree.o geomutils.o mcextract.o net.o captomc.o -lm
[hemraj@localhost c]$ cd ../rundir
[hemraj@localhost rundir]$ ../c/extract -nf nets_10.nets -t -g2.0
(Statistical Parasitic Extractor):
Current time Wed Jan 8 17:54:17 2014
    Capacitance extraction mode: TOTAL Conductors = 36
    Conductors = 36
Ground Planes = 1
    Dielectric planes = 1
Input file: nets_10.nets
Output file: nets_10.nets.extract_summary_total
Log file: Extract.log.3020
            DONE
DONE ...
[hemraj@localhost rundir]$ ls -rtl
total 24
-rwxr-xr-x. 1 hemraj hemraj 2279 Apr 8 2006 nets_10.nets
-rwxr-xr-x. 1 hemraj hemraj 168 Apr 16 2006 cube.nets.extract_summary_total
-rwxr-xr-x. 1 hemraj hemraj 727 Jan 7 19:26 Extract.log.3025
-rw-rw-rr-. 1 hemraj hemraj 717 Jan 8 15:44 Extract.log.3014
  rwxr-xr-x. 1 nemraj nemraj
rwxr-xr-x. 1 hemraj hemraj
rwxr-xr-x. 1 hemraj hemraj
rw-rw-r--. 1 hemraj hemraj
rwxr-xr-x. 1 hemraj hemraj
rw-rw-r--. 1 hemraj hemraj
                                                                         551 Jan
717 Jan
                                                                                              8 17:54 nets_10.nets.ext
8 17:54 Extract.log.3020
 [hemraj@localhost rundir]$
  ☐ hemraj@localhost:~/D...
```

Figure 2: All Input Parameters

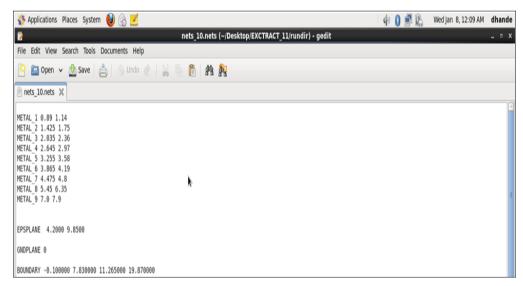
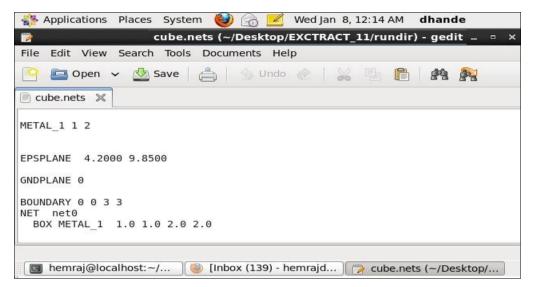


Figure 3: Selected Metals with Dimensions

Here different nets are selects for 10 metals and system calculate the cube according to the mean value of electrostatic theorem for calculation of different potential around the cube and provide the resultant values as shown in figure 4.



**Figure 4: Extracted Cube Parameters** 

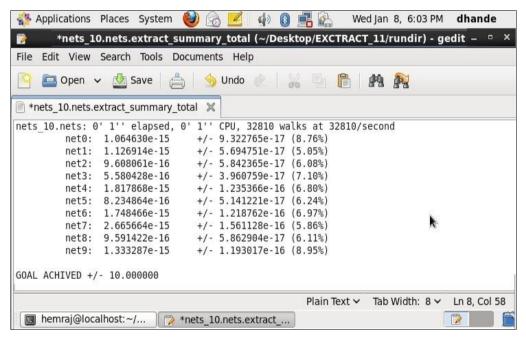


Figure 5: Result and Extracted Capacitance

The first column of Figure 5 shows 10 different nets named from net0 to net9, second column shows extracted capacitance from nets in terms of  $10^{-15}$  Farad. The resultant statistically parameter extraction along with capacitance from the 10 different metal conductors are achieved at final output.

#### CONCLUSIONS

Capacitance extraction from the VLSI chip or ICs is quite difficult task. The Monte Carlo algorithm is used for extraction of capacitance because it is comparatively faster and can handle large design than rest of techniques which requires meshing of wires. Monte Carlo algorithm followed by random walk process which helps to calculate the mutual capacitance between the two conductors. Finally experimentation results gives extraction of the capacitance from selected ten conductors with reference plane and dielectric plane. The accurate extraction of capacitance will help to improve the design and performance of the chip or ICs.

### **REFERENCES**

- 1. E. Aykut Dengi & Ronald A. Rohrer, "Boundary Element Method Macromodels for 2-D Hierarchical Capacitance Extraction", Design Automation Conferenc, pp.218-223, June 1998.
- 2. Asim Husain, "Models For Interconnect Capacitance Extraction", IEEE 2<sup>nd</sup> International Symposium on Quality Electronic Design, pp.167-172, March 2001.
- 3. Shabbir H. Batterywala & Madhav P. Desai, "Variance Reduction in Monte Carlo Capacitance Extraction", Proceedings of 18<sup>th</sup> International Conference on VLSI Design January 2005.
- 4. Genlong Chen, Hengliang Zhu, Tao Cui, Zhiming Chen, Xuan Zeng, wie Cai, "Par AFEM Cap: A Parallel Adaptive Finite-Element Method for 3-D VLSI Interconnect Capacitance Extraction" IEEE Transactions on Microwave Theory and Techniques, February 2012.
- 5. Jayant N Jere, Yannick L, Le Coz, "An Improved Floating Random-Walk Algorithm for solving the Multi-Dielectric Dirichlet Problems", IEEE Transactions on Microwave Theory and Techniques, Vol. 14, February 1993.
- 6. Taotao Lu, Zeyi Wang and Wenjianyu, "Hierarchical Block Boundary Element Method (HBBEM): A Fast Field Solver For 3-D Capacitance Extraction" IEEE Transactions on Microwave Theory and Techniques, Vol. 52, January 2004.
- L. Le Coz, H.J. Greub and R.B. Iverson "Performance of Random Walk Capacitance Extractors for IC Interconnects: A Numerical Study" Sematch Report, March 1995.
- 8. Christian P.Robert and George Casella, Monte Carlo statisticalmethods, Springer, New York, 1999.
- 9. Nidhi Sawhney, Shabbir Batterywala, Narendra Shenoy, and Richar Rudell, "Parallelizing a statistical capacitance extractor," Proceedings of VLSI Design and Test, pp. 253–267, 2004.
- K. Nabors and J. White, "Fast Cap: A multi poleaccelerated 3-D capacitance extraction program," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, volume. 10, no. (11),pp. 1447–1459, November 1991.
- 11. Xiaochun Nie, Lewei Li, and Ning Yuan, "A precorrected-FFT approach for capacitance extraction of general three-dimensional structures," IEEE Antennas and Propagation Society International Symposium, volume 3, pp. 28–31, July 2001.